

FIGURE 1

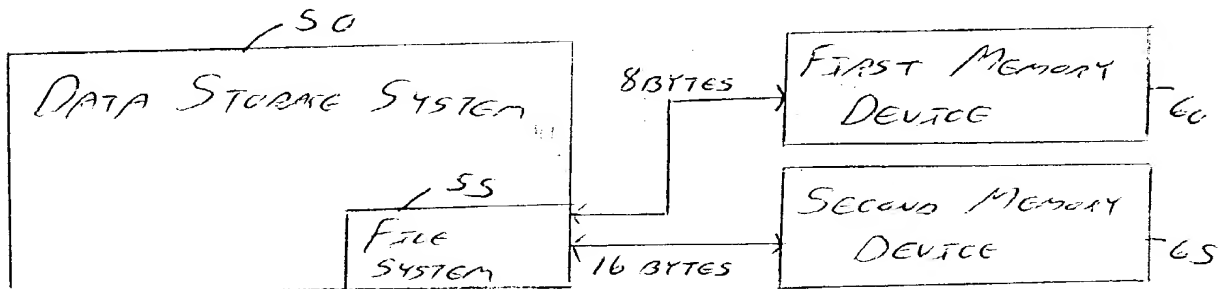


FIGURE 3

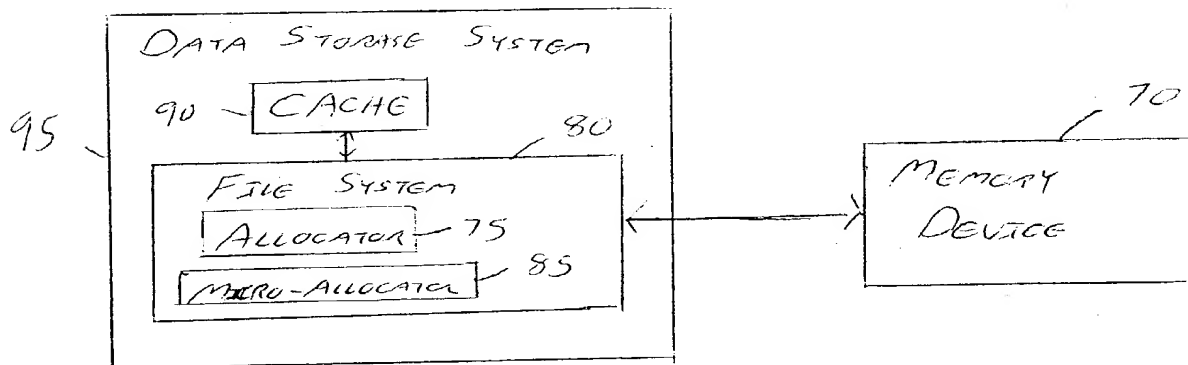


FIGURE 5

MEMORY
ARRAY

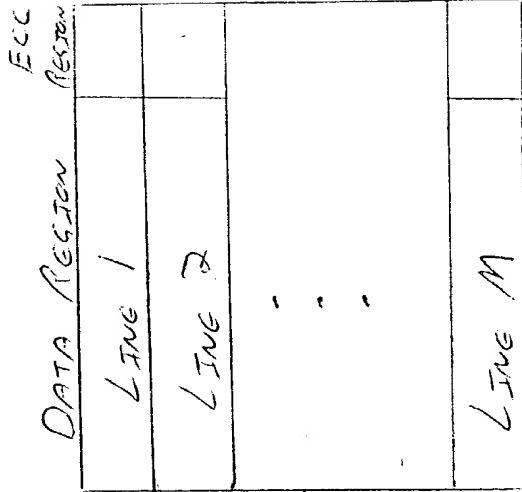
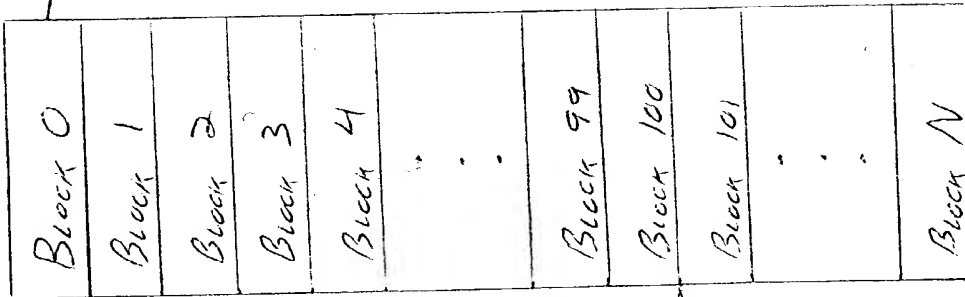


Figure 2

DATA REGION					ECC REGION				
1	0	0	1	1	0	0	1	0	0
1	0	0	1	0	0	1	0	0	1

Figure 4A

DATA REGION					ECC REGION				
1	0	1	0	1	0	1	0	1	0
1	0	1	0	1	0	1	0	0	0

Figure 4B

DATA REGION					ECC REGION				
1	0	1	1	0	1	1	1	1	0
1	0	1	1	0	1	1	1	0	1

Figure 4C

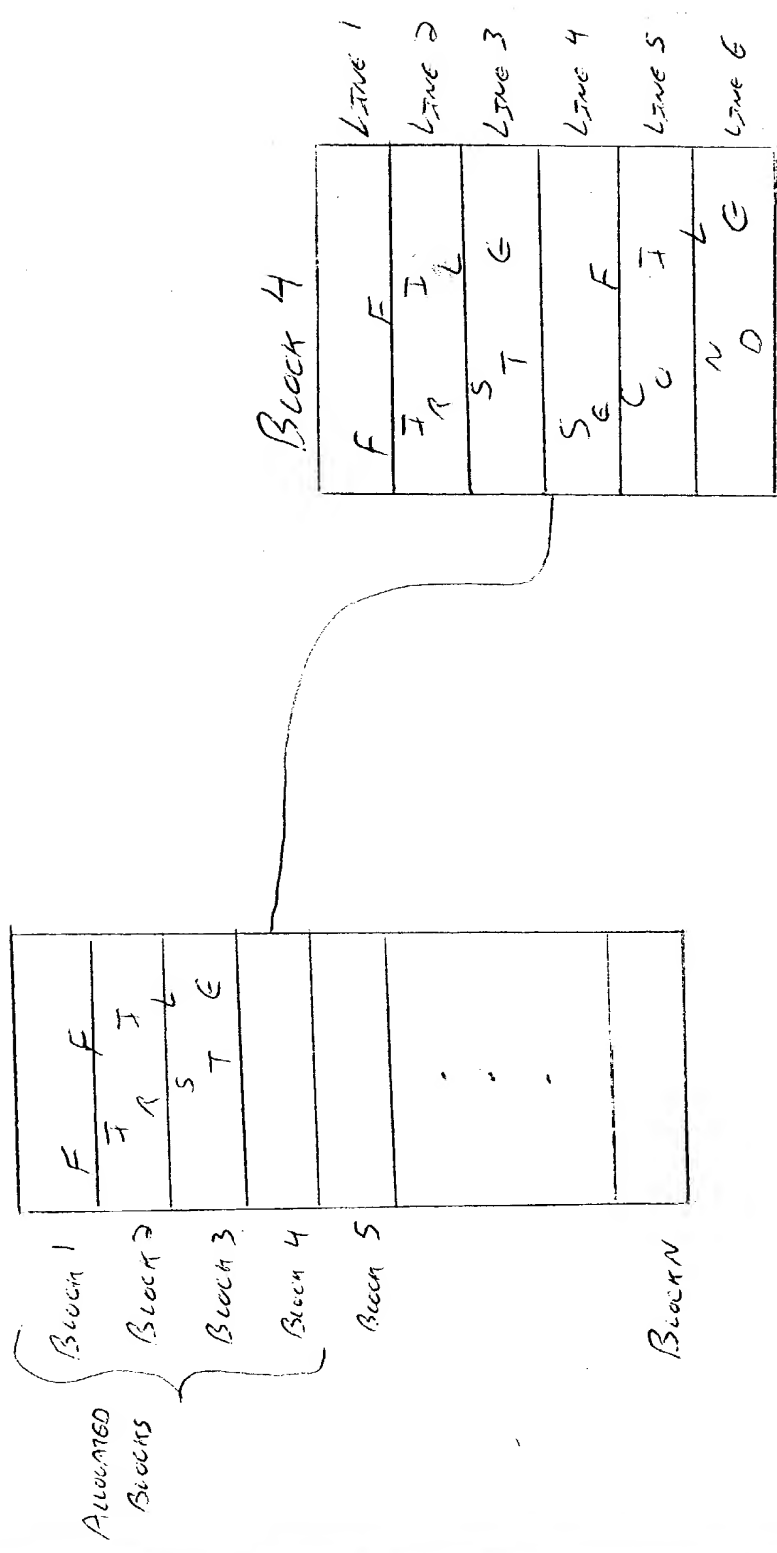


Figure 6

LINE 1	
LINE 2	
LINE 3	
LINE 4	
LINE 5	
LINE 6	RESERVED FOR FREE STRUCTURES

FIGURE 7A

LINE 1	
LINE 2	F
LINE 3	F L
LINE 4	E
LINE 5	
LINE 6	FREE STRUCTURES

SL
Faintly

LINE 1	F ₁ R F ₁ L
LINE 2	'S T E
LINE 3	FILE STRUCTURES
LINE 4	FOR FIRST FILE
LINE 5	
LINE 6	RESERVED FOR "FILE" STRUCTURES OF SECOND FILE

Figure 7c

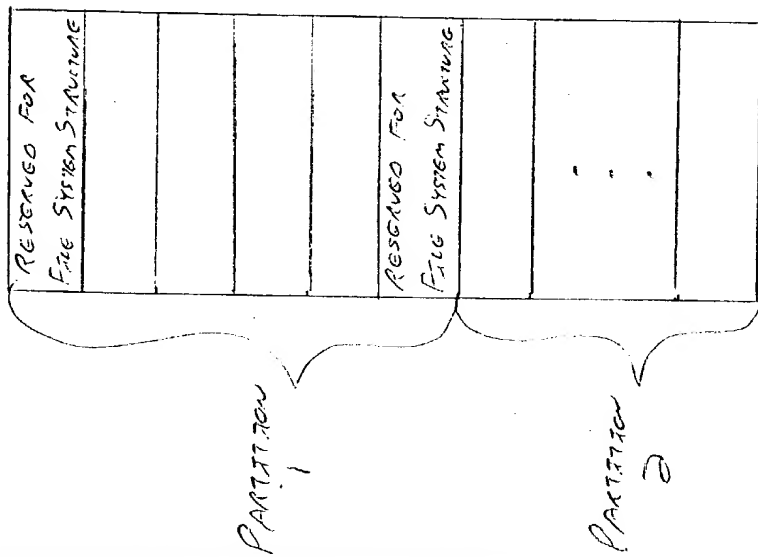


FIGURE 8A

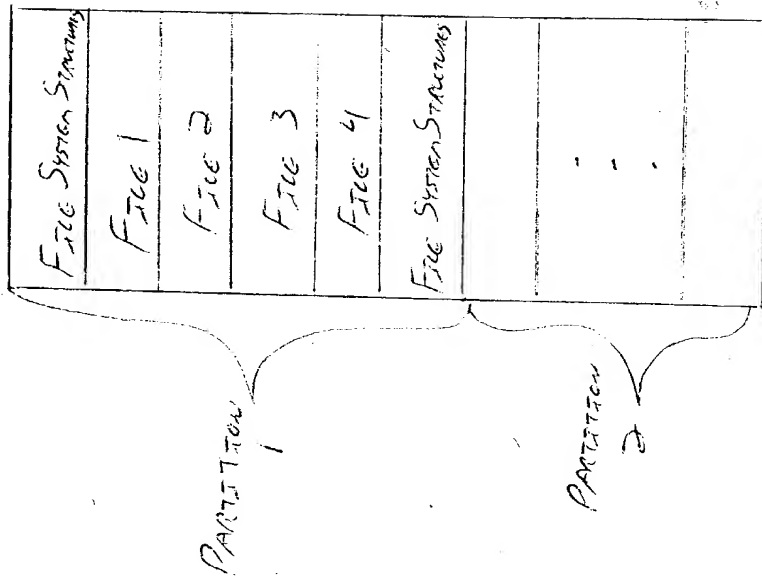


FIGURE 8B

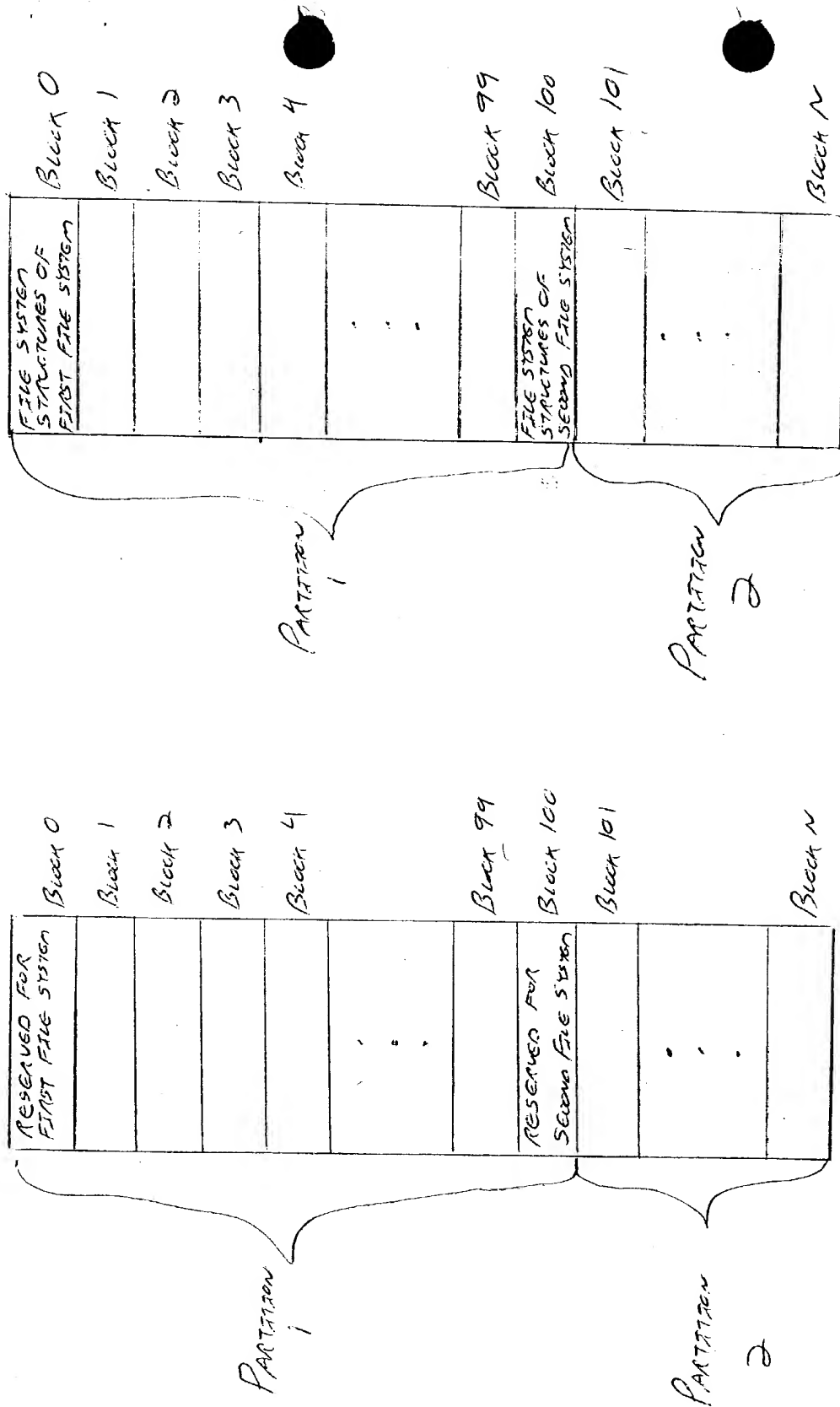


FIGURE 9A

FIGURE 9B

[illegible]

1	0	0	0	0	0
0	0	0	0	0	0
1	0	0	0	0	0
1	0	0	0	0	0

Figure 10A

1	1	0	0	0	0
1	1	1	0	0	0
1	1	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0

Figure 103

1	1	0	0	1	0
1	1	1	0	0	0
1	1	0	0	0	0
1	1	0	1	0	0
1	0	0	1	0	0
1	0	0	0	1	0

Figure 10c

200

Memory Device

210

Memory
Cells

P ECC CODE
BITS

ECC CODE CIRCUITRY

230

ECC CODE GENERATOR

ECC CODE DECODER

240

K STORED
BITS

220

N DATA BITS

N CORRECTED DATA
BITS

Figure 11